25 Spring ECEN 607: Advanced Analog Circuit Tech

Design Post-lab Report

Lab4: Op Amp Design - I

Name: Yu-Hao Chen

UIN:435009528

Section:601

Professor: Jose Silva-Martinez

TA: Yoon, Sung J

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| NFETMX current density (L=1.4u) |
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| PFETMX current density (L=1.4u) |

1. Simulate the circuit from the prelab and adjust the transistor sizes accordingly until all specifications are met. Provide necessary plots such that you clearly show the specs are met. The output swing specification should be tested with a transient simulation.

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| Vcm (Vin Dc operation )range |
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| DC gain= 82dB & GBW= 30.19M Hz |
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| Vo= 0.4-0.4 sin, /AV=13.172k, Vi=30.387u @1k |
|  |
| Output swing |
|  |
| PM= 56.11 deg |
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| Power Dissipated= 293uW |
|  |
| Input referred noise |
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1. Run a statistical simulation (Monte Carlos) and provide the worst-case DC Gain, GBW, Phase Margin and input referred noise. You do not have to adjust the design if the specs are not met. Comment the results.

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1. Configure a unity-gain buffer and apply a differential pulse of 1 KHz, 0.4 Vpp. Show the screen shots and provide comments on the step response; 30% and 1% settling time? Ringing? Comment on the results.

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30% settling time = Vo\*0.3

1. Provide a comparison table of hand-calculated vs. final transistor sizes including the required specs vs. simulated specs.

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| --- | --- | --- |
| Pre (including RL 100k) | Post (without RL 100k) | Spec |
| M1&M2: 6.28m/1.4u | M1&M2:220u/1.4u | Av0: 82.86dB |
| M3&M4: 1.82m/1.4u | M3&M4: 24.07u/1.4u | GBW: 38.17M |
| M5: 9.2m/1.4u | M5: 121.49u/1.4u | PM: 55.48 |
| M6&M7:9.2m/1.4u | M6&M7:121.49u/1.4u | Noise: 34.64u |
| M9: 1.82m/1.4u | M9: 48.14u/1.4u | Swing: |
|  |  | Power: 293.7uW |

1. Conclusion

The **Cascode NFETMX Amplifier** is a high-gain, high-bandwidth design widely used in analog circuits due to its superior performance in voltage gain, output impedance, and frequency response. It combines a **common-source (CS)** stage with a **common-gate (CG)** configuration, leveraging the strengths of both configurations. Just as the usual amplifier, for the low noise we need to increase the Id and Gm of the input stage. The stability will be stable compare to other amplifier because the dominant pole at output is dominate by CL which is large than pole2 (Cgs Cgd…), so the two will be separate widely.